ABSTRACT OF THE DISCLOSURE

A leading one correction circuit receives a significand from a floating point adder and a corresponding leading one prediction from a leading one predictor, and determines if the leading one prediction is correct. In one embodiment, the leading one prediction is a one hot vector having the same number of bits as the significand, with the set bit in the position predicted to have the leading one. In such an embodiment, the leading one correction circuit may perform a bitwise AND of the significand and leading one prediction, and the result of the bitwise AND may be ORed to generate a signal indicating whether or not the prediction is correct. In one implementation, the leading one correction circuit may operate concurrent with a shift of the significand in response to a shift amount indicated by the leading one prediction.